IN THE CLAIMS:

Amend claims 1, 3, 7 and 11 and add new claims 13-24 as shown in the following listing of claims, which replaces all previous listings and versions of claims in this application.

1. (currently amended) A vertical MOS transistor comprising:

a semiconductor substrate of a first conductivity type;

an epitaxial growth layer of the first conductivity type formed on the semiconductor substrate;

a body region of a second conductivity type formed on the epitaxial growth layer;

a heavily doped body contact region of the second conductivity type formed on a part of a surface of the body region;

a heavily doped source region of the first conductivity type formed on a part of the surface of the body region that is not covered with the heavily doped body contact region;

a silicon trench piercing the body region and the heavily doped source region to reach an inner part of the epitaxial growth layer;

a gate insulating film formed along side wall surfaces and bottom surfaces of the silicon trench;

a heavily doped polycrystalline silicon gate buried in the silicon trench over the gate insulating film to a level of the heavily doped source region;

an intermediate insulating film formed on the heavily doped polycrystalline silicon gate in the silicon trench to reach a surface of the semiconductor substrate;

~~an insulator~~ side spacers disposed on the side walls of the silicon trench and above the heavily doped polycrystalline silicon gate;

a metallic source electrode having a flat surface in contact with the intermediate insulating film, the heavily doped source region, and the heavily doped body contact region; and

a metallic drain electrode connected to a rear surface of the semiconductor substrate.

2. (canceled).

3. (currently amended) A vertical MOS transistor according to claim 1; wherein the ~~insulator~~ side spacers disposed on the side walls of the silicon trench ~~comprises~~ comprise a silicon nitride film.

4. (previously presented) A vertical MOS transistor according to claim 3; wherein the heavily doped polycrystalline silicon gate is buried 0.5 μm to 1.0 μm down from a top of the silicon trench.

5. (previously presented) A vertical MOS transistor according to claim 1; wherein the heavily doped polycrystalline silicon gate is buried 0.5 μm to 1.0 μm down from a top of the silicon trench.

6. (canceled).

7. (currently amended) A vertical MOS transistor comprising:

a semiconductor substrate;

an epitaxial growth layer disposed on the semiconductor substrate;

a body region disposed on the epitaxial growth layer;

a heavily doped body contact region disposed on a part of a surface of the body region;

a heavily doped source region disposed on a part of the surface of the body region on which the heavily doped body contact region is not disposed;

a silicon trench extending through the heavily doped source region and the body region and extending into the epitaxial growth layer, the silicon trench having sidewall surfaces and a bottom surface;

a gate insulating film disposed on the sidewall and bottom surfaces of the silicon trench;

a heavily doped polycrystalline silicon gate disposed in the silicon trench over the gate insulating film and extending below a surface formed by the body region and the heavily doped body contact region;

an intermediate insulating film disposed on the heavily doped polycrystalline silicon gate in the silicon trench so as to reach the surface formed by the body region and the heavily doped body contact region; and

~~an insulator~~ side spacers disposed on the sidewalls of the silicon trench and above the heavily doped polycrystalline silicon gate.

8. (previously presented) A vertical MOS transistor according to claim 7; further comprising a metallic source electrode having a generally planar surface disposed in contact with the intermediate insulating film, the heavily doped source region, and the heavily doped body contact region.

9. (previously presented) A vertical MOS transistor according to claim 8; wherein the surface of the semiconductor substrate comprises a first surface; and further comprising a metallic drain electrode connected to a second surface of the semiconductor substrate opposite to the first surface thereof.

10. (previously presented) A vertical MOS transistor according to claim 7; wherein each of the semiconductor substrate, the epitaxial growth layer, and the heavily doped source region have a first conductivity type; and wherein each of the body region and the heavily doped body contact region have a second conductivity type different from the first conductivity type.

11. (currently amended) A vertical MOS transistor according to claim 7; wherein the ~~insulator comprises~~ side spacers comprise a silicon nitride film.

12. (previously presented) A vertical MOS transistor according to claim 7; wherein a distance from the surface formed by the body region and the heavily doped body contact region to an upper surface of the heavily doped polycrystalline silicon gate disposed in the silicon trench is in the range of 0.5 μm to 1.0 μm.

13. (new) A vertical MOS transistor according to claim 1; wherein the intermediate insulating film is formed directly on the heavily doped polycrystalline silicon gate and the side spacers.

14. (new) A vertical MOS transistor according to claim 1; wherein the side spacers are disposed between the gate insulating film and the intermediate insulating film.

15. (new) A vertical MOS transistor according to claim 1; wherein the side spacers and the intermediate insulating film are made of different materials.

16. (new) A vertical MOS transistor according to claim 1; wherein the side spacers are separate and independent from the gate insulating film and the intermediate insulating film.

17. (new) A vertical MOS transistor according to claim 7; wherein the intermediate insulating film is formed directly on the heavily doped polycrystalline silicon gate and the side spacers.

18. (new) A vertical MOS transistor according to claim 7; wherein the side spacers are disposed between the gate insulating film and the intermediate insulating film.

19. (new) A vertical MOS transistor according to claim 7; wherein the side spacers and the intermediate insulating film are made of different materials.

20. (new) A vertical MOS transistor according to claim 7; wherein the side spacers are separate and independent from the gate insulating film and the intermediate insulating film.

21. (new) A vertical MOS transistor comprising:

a semiconductor substrate of a first conductivity type;

an epitaxial growth layer of the first conductivity type formed on the semiconductor substrate;

a body region of a second conductivity type formed on the epitaxial growth layer;

a heavily doped body contact region of the second conductivity type formed on a part of a surface of the body region;

a heavily doped source region of the first conductivity type formed on a part of the surface of the body region that is not covered with the heavily doped body contact region;

a silicon trench piercing the body region and the heavily doped source region to reach an inner part of the epitaxial growth layer;

a gate insulating film formed along side wall surfaces and bottom surfaces of the silicon trench;

a heavily doped polycrystalline silicon gate buried in the silicon trench over the gate insulating film to a level of the heavily doped source region;

an intermediate insulating film formed on the heavily doped polycrystalline silicon gate in the silicon trench to reach a surface of the semiconductor substrate;

an insulator separate and independent from the gate insulating film and the intermediate insulating film and disposed on the side walls of the silicon trench and above the heavily doped polycrystalline silicon gate;

a metallic source electrode having a flat surface in contact with the intermediate insulating film, the heavily doped source region, and the heavily doped body contact region; and

a metallic drain electrode connected to a rear surface of the semiconductor substrate.

22. (new) A vertical MOS transistor according to claim 21; wherein the insulator and the intermediate insulating film are made of different materials.

23. (new) A vertical MOS transistor according to claim 22; wherein the insulator comprises a nitride film.

24. (new) A vertical MOS transistor according to claim 23; wherein the intermediate insulating film comprises an oxide film.